PATENT
Attorney Docket No. 03180.0278

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:	)	
	)	
Ryoichi INANAMI et al.	)	Group Art Unit: 2881
	)	
Application No.: 09/817,270	)	Examiner: Phillip A. Johnston
	)	
Filed: March 27, 2001	)	
	)	
For: EXPOSURE PATTERN DATA GENERATION APPARATUS ASSOCIATED WITH STANDARD CELL LIBRARY AND CHARGED BEAM EXPOSURE	)	Confirmation No.: 7690

Mail Stop Appeal Brief--Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

TRANSMITTAL OF APPEAL BRIEF (37 C.F.R. 41.37)

Transmitted herewith is the APPEAL BRIEF in this application with respect to the Notice of Appeal filed on November 27, 2006.

This application is on behalf of

☐ Small Entity ☒ Large Entity

Pursuant to 37 C.F.R. 41.20(b)(2), the fee for filing the Appeal Brief is:

☐ $250.00 (Small Entity)

☒ $500.00 (Large Entity)

TOTAL FEE DUE:

Appeal Brief Fee	$500.00
Extension Fee (if any)	$0.00

Total Fee Due $500.00

☒ Enclosed is a check for $500.00 to cover the above fees.

PETITION FOR EXTENSION. If any extension of time is necessary for the filing of this Appeal Brief, and such extension has not otherwise been requested, such an extension is hereby requested, and the Commissioner is authorized to charge necessary fees for such an extension to our Deposit Account No. 06-0916. A duplicate copy of this paper is enclosed for use in charging the deposit account.

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: January 26, 2007

By: _____
Darrell D. Kinder, Jr.
Reg. No. 57,460

PATENT
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	
Ryoichi INANAMI et al.	Group Art Unit: 2881
Application No.: 09/817,270	Examiner: Phillip A. Johnston
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Attention: Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

APPEAL BRIEF UNDER RULE § 41.37

In support of the Notice of Appeal filed November 27, 2006, further to 37 C.F.R. § 41.37, Appellants present this Appeal Brief and enclose herewith a check for the fee of $500.00 required under 37 C.F.R. § 41.20(b)(2).

This Appeal is filed to appeal the rejections of claims 1-34 set forth in the Office Action mailed May 26, 2006.

This Appeal Brief is being timely submitted within two (2) months of the November 27, 2006, filing date of the Notice of Appeal.

If any additional fees are required or if the enclosed payment is insufficient, Appellants request that the required fees be charged to Deposit Account No. 06-0916.

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I. REAL PARTY IN INTEREST

The real party in interest is Kabushiki Kaisha Toshiba, a corporation of Japan, and the assignee of the entire right, title, and interest in the application.

II. RELATED APPEALS AND INTERFERENCES

There are currently no other appeals or interferences, of which Appellants, Appellants' legal representative, or the Assignee is aware, that will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1-34 are pending in the above-captioned patent application, and are the subject of this appeal.

In the Office Action mailed May 26, 2006, the Examiner rejected claims 1-34 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,546,544 to Kawakami ("Kawakami") in view of U.S. Patent No. 6,225,025 to Hoshino ("Hoshino").

The claims on appeal are set forth in Section VIII entitled "Claims Appendix."

IV. STATUS OF AMENDMENTS

Appellants filed an Amendment on October 5, 2005, which has been entered.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The invention, as recited in independent claim 1 is directed to a charged beam exposure (Fig. 7) for delineating patterns of systems on substrates (Fig. 7, 47) to describe the systems in logic expressions (page 13, lines 5-15), to convert the logic expressions into connections of standard cells (page 13, lines 15-20), and to delineate patterns of the standard cells on the substrates (Fig. 7, 47; page 13, lines 20-22). The disclosed exposure includes a beam generation source generating charged beams (Fig. 7, 41), and Character Projection (CP) apertures (Fig. 7, 44) having shaping holes of the charged beams (Fig. 7, 4; page 9, lines 24-25) having shapes of one hundred or more characters having shapes of the standard cells (page 24, lines 21-25).

The disclosed exposure also includes standard cell library recording means (Fig. 7, 102) for recording a standard cell library having an information configured to design the patterns of the systems by using the standard cells having functions (page 13, lines 20-22), shapes of outlines (page 12, lines 22-23), and input/output positions of the standard cells (page 12, line 23). The standard cell library recording means is also for recording the standard cell library having first placement positions of the shaping holes on said CP apertures related to the standard cells corresponding to the shaping holes (Fig. 7, 4; page 12, lines 28-34).

In addition, the disclosed exposure includes Character Projection (CP) aperture decision means (Fig. 8, 84) for conducting logic synthesis for the CP apertures (Fig. 8, 86) using only the standard cells corresponding to the shaping holes placed on first placement positions on the respective CP apertures (Fig. 7, 44; page 11, lines 14-16,

page 17, lines 13-14). The CP aperture decision means is also for selecting one of the CP apertures for which the logic synthesis is conducted (page 11, lines 16-18) by using only the standard cells on the one of the CP apertures (page 19, lines 1-6), which satisfies designated constraints of the systems (page 11, line 20), and which has the highest throughput in delineating one of the patterns of the systems on the substrates by using only the standard cells on the one of the CP apertures (page 23, lines 1-5). The CP aperture decision means is also for conducting logic synthesis again for the respective CP apertures without a constraint on using only the standard cells on the one of the CP apertures (page 20, lines 2-5), and for selecting one of the CP apertures, for which the logic synthesis is conducted again (page 20, lines 15-17), and which has a throughput higher than a desired throughput in delineating one of the patterns of the systems on the substrates based on the standard cell library (page 21, lines 6-20).

The disclosed exposure also includes placement and routing means (Fig. 8, 89) for calculating second placement positions of the standard cells on the substrates (page 11, lines 2-5), the standard cells corresponding to the shaping holes provided on the selected one of the CP apertures based on the standard cell library (page 11, lines 24-27), and pattern data recording means (Fig. 8, 103) for recording second placement positions of the standard cells on the substrates (page 11, line 35 - page 12, line 2), the second placement positions associated with the standard cells corresponding to the first placement positions on the selected one of the CP apertures (page 11, line 35 - page 12, line 2).

The exposure further includes a character select deflector (Fig. 7, 81) irradiating the charged beams onto the shaping holes (Fig. 7, 4; page 10, lines 2-3) at the first placement positions on the selected one of the CP apertures (Fig. 7, 44; page 10, lines 8-13), and an objective deflector (Fig. 7, 46) irradiating the charged beams onto the second placement positions on the substrates (Fig. 7, 47; page 10, lines 8-13).

The invention, as recited in independent claim 7 is directed to an exposure pattern data generation apparatus (Fig. 7) for delineating patterns of systems on substrates to describe the systems in logic expressions (page 13, lines 5-15), to convert the logic expressions into connections of standard cells (page 13, lines 15-20), and to delineate patterns of the standard cells on the substrates (Fig. 7, 47; page 13, lines 20-22). The exposure pattern data generation apparatus includes Character Projection (CP) aperture creation means for creating CP apertures having shaping holes (Fig. 7, 44, 4; page 9, lines 24-25) corresponding to one hundred or more characters having shapes of the standard cells (page 24, lines 21-25).

The exposure pattern data generation apparatus also includes standard cell library recording means (Fig. 7, 102) for recording a standard cell library having an information configured to design the patterns of the systems by using the standard cells having functions (page 13, lines 20-22), shapes of outlines (page 12, lines 22-23), and input/output positions of the standard cells (page 12, line 23). The standard cell library recording means are also for recording the standard cell library having first placement positions of the shaping holes on said CP apertures related to the standard cells corresponding to the shaping holes (Fig. 7, 4; page 12, lines 28-34).

In addition, the exposure pattern data generation apparatus includes Character Projection (CP) aperture decision means (Fig. 8, 84) for conducting logic synthesis for the CP apertures (Fig. 8, 86) using only the standard cells corresponding to the shaping holes placed on first placement positions on the respective CP apertures (Fig. 7, 44; page 11, lines 14-16, page 17, lines 13-14). The CP aperture decision means are also for selecting one of the CP apertures for which the logic synthesis is conducted (page 11, lines 16-18) by using only the standard cells on the one of the CP apertures (page 19, lines 1-6), which satisfies designated constraints of the systems (page 11, line 20), and which has the highest throughput in delineating one of the patterns of the systems on the substrates by using only the standard cells on the one of the CP apertures (page 23, lines 1-5). The CP aperture decision means is also for conducting logic synthesis again for the respective CP apertures without a constraint on using only the standard cells on the one of the CP apertures (page 20, lines 2-5). Moreover, the CP aperture decision means is further for selecting one of the CP apertures, for which the logic synthesis is conducted again (page 20, lines 15-17), and which has a throughput higher than a desired throughput in delineating one of the patterns of the systems on the substrates based on the standard cell library (page 21, lines 6-20).

The exposure pattern data generation apparatus also includes placement and routing means (Fig. 8, 89) for calculating second placement positions of the standard cells on the substrates (page 11, lines 2-5), the standard cells corresponding to the shaping holes provided on the selected one of the CP apertures based on the standard cell library (page 11, lines 24-27), and pattern data recording means (Fig. 8, 103) for

recording second placement positions of the standard cells on the substrates (page 11, line 35 - page 12, line 2, the second placement positions associated with the standard cells corresponding to the first placement positions on the selected one of the CP apertures (page 11, line 35 - page 12, line 2).

The invention, as recited in independent claim 15, is directed to an exposure pattern data generation method (Figs. 8, 9, 14) for delineating patterns of systems on substrates to describe the systems in logic expressions (page 13, lines 5-15), to convert the logic expressions into connections of standard cells (page 13, lines 15-20), and to delineate patterns of the standard cells on the substrates (Fig. 7, 47; page 13, lines 20-22). The exposure pattern data generation method includes creating Character Projection (CP) apertures (Fig. 7, 44) having shaping holes corresponding to one hundred or more characters having shapes of the standard cells (page 9, lines 24-25, page 24, lines 21-25).

The exposure pattern data generation method also includes recording a standard cell library (Fig. 8, 101) having an information configured to design the patterns of the systems by using the standard cells having functions (page 13, lines 20-22), shapes of outlines (page 12, lines 22-23), and input/output positions of the standard cells (page 12, line 23), and recording the standard cell library having first placement positions of the shaping holes on said CP apertures related to the standard cells corresponding to the shaping holes (page 12, lines 28-34).

In addition, the exposure pattern data generation method includes conducting logic synthesis for the Character Projection (CP) apertures (Fig. 8, 86) using only the

standard cells corresponding to the shaping holes placed at first placement positions on the respective CP apertures on the substrate based on the standard cell library (page 11, lines 14-16, page 17, lines 13-14), and selecting one of the CP apertures for which the logic synthesis is conducted (page 11, lines 16-18) by using only the standard cells on the one of the CP apertures (page 19, lines 1-6), which satisfies designated constraints of the systems (page 11, line 20), and which has the highest throughput in delineating one of the patterns of the systems on the substrates by using only the standard cells on the one of the CP apertures (page 23, lines 1-5).

The exposure pattern data generation method also includes conducting logic synthesis again for the respective CP apertures without a constraint on using only the standard cells on the one of the CP apertures (Fig. 14 S17,; page 20, lines 2-5), and selecting one of the CP apertures, for which the logic synthesis is conducted again (page 20, lines 15-17), and which has a throughput higher than a desired throughput in delineating one of the patterns of the systems on the substrates from the CP apertures on the substrates based on the standard cell library (page 21, lines 6-20).

The exposure pattern data generation method further includes calculating second placement positions of the standard cells on the substrates (page 11, lines 2-5), the standard cells corresponding to the shaping holes provided on the selected one of the CP apertures on the substrates based on the standard cell library (page 11, lines 24-27), and recording second placement positions of the standard cells on the substrates (page 11, line 35 - page 12, line 2), the second placement positions

associated with the standard cells corresponding to the first placement positions on one of the selected CP apertures (page 11, line 35 - page 12, line 2).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Claims 1-34 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kawakami in view of Hoshino.

VII. ARGUMENT

A. Introduction

Each claim of this patent application is separately patentable and, upon issuance of a patent, will be entitled to a separate presumption of validity under 35 U.S.C. § 282. That is, each of claims 1-34 should be considered individually in light of the arguments against the Examiner's rejections.

B. Detailed Arguments

1. The rejection of claims 1-34 under 35 U.S.C. § 103(a) as being unpatentable over Kawakami in view of Hoshino should be reversed.

The rejection of claims 1-34 under 35 U.S.C. § 103(a) as being unpatentable over Kawakami in view of Hoshino should be reversed because no *prima facie* case of obviousness has been established.

To establish a *prima facie* case of obviousness under 35 U.S.C. § 103(a), each of three requirements must be met. First, the reference or references, taken alone or combined, must teach or suggest each and every element recited in the claims. Second, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to combine the references in a manner resulting in the claimed invention. Third, a reasonable expectation of success must exist. Moreover, each of the three requirements must "be found in the prior art, and not be based on applicant's disclosure." *See* MPEP § 2143, 8th Ed. (Rev. 5), August, 2006.

At least the first essential element for establishing a *prima facie* case of obviousness has not been met. Specifically, neither Kawakami nor Hoshino, whether taken alone or in combination, teach or suggest every element recited in claims 1-34.

In the Final Office Action mailed May 26, 2006, the Examiner initially asserts that Kawakami teaches all of the elements recited in claims 1-34 with the exception of elements related to "the use of standard cells on CP apertures listed in an order of frequency of use according to a difference between a VSB shot number and a CP shot number as recited in claims 20-23, 25, 27, 29-31, and 33." Final Office Action, page 12 (emphasis added). The Examiner thus asserts that Kawakami teaches or suggests every element recited in independent claims 1, 7, and 15. The Examiner's assertion, however, is incorrect. As discussed *infra*, Kawakami fails to teach or suggest every element recited in independent claims 1, 7, and 15.

For example, Kawakami fails to teach or suggest "conducting logic synthesis for the CP apertures [and] selecting one of the CP apertures ... which has the highest throughput in delineating one of the patterns," as recited in independent claims 1, 7, and 15. Kawakami specifically teaches:

> generating a pattern group for each layer of the integrated circuit including a plurality of the basic elements; analyzing the degree of frequency at which each basic element is used in the integrated circuit; selecting from the pattern group a pattern used as a plurality of the block patterns based on the analyzed degree of frequency at which each basic element is used... (col. 5, lines 28-35)

wherein

> by reference to the cell reference frequency information 75 and the system restraint information/mask restraints 72, the

> cells to be changed to masks are determined thereby to produce a mask layout A76 (col. 8, lines 17-20).

However, neither this portion of Kawakami, nor any other portion, constitutes a teaching or suggestion as to "selecting one of the CP apertures ... which has the highest throughput," as recited in independent claims 1, 7, and 15. Kawakami thus fails to teach or suggest an exposure, an apparatus or a method including "conducting logic synthesis for the CP apertures [and] selecting one of the CP apertures ... which has the highest throughput in delineating one of the patterns," as recited in independent claims 1, 7, and 15.

Kawakami also fails to teach or suggest a combination including "conducting logic synthesis again [and] selecting one of the CP apertures ... which has a throughput higher than a desired throughput in delineating one of the patterns," as recited in independent claims 1, 7, and 15. Despite the Examiner's earlier assertion that Kawakami teaches each and every element recited in independent claims 1, 7, and 15 (see *supra*), the Examiner contradicts himself, conceding that Kawakami fails to teach or suggest this element. The Examiner specifically states that "neither ... nor Kawakami (544) constrain the design of subsequent devices to standard cell layouts previously selected for any other device design i.e., when 'conducting logic synthesis again', as recited in claims 1, 7, and 15." Office Action, page 8 (emphasis added). Accordingly, even by the Examiner's own admission, Kawakami fails to teach or suggest a combination including "conducting logic synthesis again [and] selecting one of the CP apertures ... which has a throughput higher than a desired throughput in delineating one of the patterns," as recited in independent claims 1, 7, and 15.

Hoshino is cited by the Examiner at page 12 of the Office Action for allegedly teaching "a method of fabricating semiconductor devices with electron beam lithography that utilizes mask's having block (CP) apertures formed using shot number analysis based on frequency of use." However, Hoshino cannot be relied upon to cure the above-noted deficiencies of Kawakami. That is, Hoshino also fails to teach or suggest a combination including at least "conducting logic synthesis for the CP apertures [and] selecting one of the CP apertures ... which has the highest throughput in delineating one of the patterns," and "conducting logic synthesis again [and] selecting one of the CP apertures ... which has a throughput higher than a desired throughput in delineating one of the pattern," as recited in independent claims 1, 7, and 15.

Hoshino teaches:

> the exposure data verifying function 12 includes a pattern data display function 20 used for displaying a pattern data, an exposure data analysis unit 21 used for carrying out an analysis of the exposure data [created] by the exposure data creation function 11, and exposure throughput calculation function 22 for calculating the throughput of the exposure data creation function... (col. 8, lines 17-24)

wherein

> the exposure data is created in the exposure data creation function 11 such that the exposure time is minimized, by reducing the exposure data size (col. 9, lines 49-51).

Hoshino can at best be characterized as teaching creating exposure data in order to minimize the exposure time. However, nothing in Hoshino constitutes a teaching or suggestion of "conducting logic synthesis for the CP apertures [and] selecting one of the CP apertures ... which has the highest throughput in delineating

one of the patterns," as recited in independent claims 1, 7, and 15. Moreover, Hoshino provides no teaching or suggestion as to "conducting logic synthesis again," and thus fails to teach or suggest "conducting logic synthesis again [and] selecting one of the CP apertures ... which has a throughput higher than a desired throughput in delineating one of the pattern," as also recited in independent claims 1, 7, and 15.

The Examiner has therefore not met an essential requirement for establishing a *prima facie* case of obviousness, specifically, that "the prior art reference (or references when combined) must teach or suggest all the claim limitations." *See* MPEP §§ 2142, 2143, and 2143.03. Since establishing a *prima facie* case of obviousness requires that the cited references teach or suggest each and every element of the claimed invention, the Examiner's 35 U.S.C. § 103(a) rejection fails on at least this point.

Appellants further submit that the rejection of claims 1-34 is improper because the Examiner has impermissibly read limitations from the specification into the claims, and has thus mischaracterized Appellants' claims. Specifically, the Examiner in applying the references against claims 1-34, asserts that based on Appellants' specification "the subject limitation refers to the steps for designing two different devices A and B, where the system constraint of designing device A using standard cells only, is subsequently removed prior to designing device B." Office Action, page 5 (emphasis added). In addition, the Examiner further asserts that Kawakami and claims 1, 7, and 15, "both perform multiple device design layouts using a stored standard cell library." Office Action, page 8.

The MPEP states that "the words of the claim must be given their plain meaning unless the plain meaning is inconsistent with the specification." MPEP § 2111.01, 8th Ed. (Rev. 5), August, 2006 (citing In re Zletz, 893 F.2d 319, 321, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989)). In giving the words their plain meaning, "it is important not to import into a claim limitations that are not part of the claim. For example, a particular embodiment appearing in the written description may not be read into a claim when the claim language is broader than the embodiment." Id. (citing Superguide Corp. v. DirecTV Enterprises, Inc., 358 F.3d 870, 875, 69 USPQ2d 1865, 1868 (Fed. Cir. 2004)).

Here, the Examiner has characterized Appellants' claims 1, 7, and 15 as defining "steps for designing two different devices A and B, where the system constraint of designing device A using standard cells only, is subsequently removed prior to designing device," admittedly based on Appellants' specification. *See* Office Action, page 5. The Examiner further asserts that such steps are taught by Kawakami or Hoshino. Id.

Appellants strongly disagree with the Examiner's characterization of Appellants' claims. Even if the Examiner could be considered correct that Appellants' specification, which merely describes an embodiment of Appellants' invention, "refers to the steps for designing two different devices A and B, where the system constraint of designing device A using standard cells only, is subsequently removed prior to designing device B," the rejection under 35 U.S.C. § 103(a) is improper for the additional reason that the Examiner has impermissibly imported limitations from the specification into claims 1, 7, and 15, and thus mischaracterized Appellants' claims 1, 7, and 15. *See* MPEP

§ 2111.01 II, 8th Ed. (Rev. 5), August, 2005 (citing In re Zletz, wherein the court held that an Examiner improperly interpreted a claim by importing limitations from the specification).

Moreover, Appellants further note that "[i]n determining the differences between the prior art and the claims, the question under 35 U.S.C. § 103 is not whether the differences themselves would have been obvious, but whether the claimed invention as a whole would have been obvious. MPEP § 2141.02 (*citing* Stratoflex, Inc. v. Aeroquip Corp., 713 F.2d 1530, 218 USPQ 871 (Fed. Cir. 1983); Schenck v. Nortron Corp., 713 F.2d 782, 218 USPQ 698 (Fed. Cir. 1983)). Here, the Examiner has not shown that independent claims 1, 7, and 15 when viewed as a whole, would have been obvious over Kawakami in view of Hoshino. For at least these additional reasons, a *prima facie* obviousness of independent claims 1, 7, and 15 has not been established.

Because no *prima facie* case of obviousness of independent claim 1 has been established, independent claims 1, 7, and 15 are therefore allowable. If an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious. In re Fine, 837 F.2d 1071, 5 U.S.P.Q. 2d 1596 (Fed. Cir. 1988). Dependent claims 2-6, 22-26, and 34 are therefore allowable at least by virtue of their dependency from allowable independent claim 1; dependent claims 8-14 and 27-29 are allowable at least by virtue of their dependency from allowable independent claim 7; and dependent claims 16-21 and 30-33 are allowable at least by virtue of their dependency from allowable independent claim 15. Therefore, the improper rejection of claims 1-34 under 35 U.S.C. § 103(a) should be reversed.

For the reasons given above, pending claims 1-34 are allowable. Appellants respectfully request that the Board reverse the Examiner's rejections.

To the extent any extension of time under 37 C.F.R. § 1.136 is required to obtain entry of this Appeal Brief, such extension is hereby respectfully requested. If there are any fees due under 37 C.F.R. §§ 1.16 or 1.17 that are not enclosed herewith, including any fees required for an extension of time under 37 C.F.R. § 1.136, please charge such fees to our Deposit Account No. 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: January 26, 2007

By: 
Darrell D. Kinder, Jr.
Reg. No. 57,460

VIII. CLAIMS APPENDIX

Claims Appendix to Appeal Brief Under Rule 41.37(c)(1)(viii)

1. A charged beam exposure for delineating patterns of systems on substrates to describe the systems in logic expressions, to convert the logic expressions into connections of standard cells, and to delineate patterns of the standard cells on the substrates, comprising:

a beam generation source generating charged beams;

Character Projection (CP) apertures having shaping holes of the charged beams having shapes of one hundred or more characters having shapes of the standard cells;

standard cell library recording means for recording a standard cell library having an information configured to design the patterns of the systems by using the standard cells having functions, shapes of outlines, and input/output positions of the standard cells, and for recording the standard cell library having first placement positions of the shaping holes on said CP apertures related to the standard cells corresponding to the shaping holes;

Character Projection (CP) aperture decision means for conducting logic synthesis for the CP apertures using only the standard cells corresponding to the shaping holes placed on first placement positions on the respective CP apertures; for selecting one of the CP apertures for which the logic synthesis is conducted by using only the standard cells on the one of the CP apertures, which satisfies designated constraints of the systems, and which has the highest throughput in delineating one of the patterns of the systems on the substrates by using only the standard cells on the

one of the CP apertures; for conducting logic synthesis again for the respective CP apertures without a constraint on using only the standard cells on the one of the CP apertures; and for selecting one of the CP apertures, for which the logic synthesis is conducted again, and which has a throughput higher than a desired throughput in delineating one of the patterns of the systems on the substrates based on the standard cell library;

placement and routing means for calculating second placement positions of the standard cells on the substrates, the standard cells corresponding to the shaping holes provided on the selected one of the CP apertures based on the standard cell library;

pattern data recording means for recording second placement positions of the standard cells on the substrates, the second placement positions associated with the standard cells corresponding to the first placement positions on the selected one of the CP apertures;

a character select deflector irradiating the charged beams onto the shaping holes at the first placement positions on the selected one of the CP apertures; and

an objective deflector irradiating the charged beams onto the second placement positions on the substrates.

2. The exposure as in claim 1, further comprising:

a first shaping aperture rectangularly shaping an irradiation pattern of one of the charged beams to said CP aperture.

3. The exposure as in claim 1, further comprising:

a demagnifying lens demagnifying the irradiation pattern of one of the charged beams on the substrate.

4. The exposure as in claim 1, wherein said standard cell library recording means further records input and output positions of signals of the standard cells.

5. The exposure as in claim 1, wherein one of the CP apertures further has an opening for a variable shaped beam (VSB).

6. The exposure as claimed in claim 1, wherein

the shaping holes have a shape of one of the standards cell having a higher frequency of use or a shape of one of the standard cells corresponding to reducing a number of shots by CP exposure.

7. An exposure pattern data generation apparatus for delineating patterns of systems on substrates to describe the systems in logic expressions, to convert the logic expressions into connections of standard cells, and to delineate patterns of the standard cells on the substrates, comprising:

Character Projection (CP) aperture creation means for creating CP apertures having shaping holes corresponding to one hundred or more characters having shapes of the standard cells;

standard cell library recording means for recording a standard cell library having an information configured to design the patterns of the systems by using the standard cells having functions, shapes of outlines, and input/output positions of the standard cells, and for recording the standard cell library having first placement positions of the shaping holes on said CP apertures related to the standard cells corresponding to the shaping holes;

Character Projection (CP) aperture decision means for conducting logic synthesis for the CP apertures using only the standard cells corresponding to the shaping holes placed on first placement positions on the respective CP apertures; for selecting one of the CP apertures for which the logic synthesis is conducted by using only the standard cells on the one of the CP apertures, which satisfies designated constraints of the systems, and which has the highest throughput in delineating one of the patterns of the systems on the substrates by using only the standard cells on the one of the CP apertures; for conducting logic synthesis again for the respective CP apertures without a constraint on using only the standard cells on the one of the CP apertures; and for selecting one of the CP apertures, for which the logic synthesis is conducted again, and which has a throughput higher than a desired throughput in delineating one of the patterns of the systems on the substrates based on the standard cell library;

placement and routing means for calculating second placement positions of the standard cells on the substrates, the standard cells corresponding to the shaping holes

provided on the selected one of the CP apertures based on the standard cell library; and

pattern data recording means for recording second placement positions of the standard cells on the substrates, the second placement positions associated with the standard cells corresponding to the first placement positions on the selected one of the CP apertures.

8. The apparatus as in claim 7, further comprising:

variable shaped beam (VSB) exposure data conversion means for converting data into data capable of being used by an exposure to conduct VSB exposure to the standard cells which cannot be subject to exposure using the shaping holes.

9. The apparatus as in claim 7, wherein

said CP aperture decision means comprises:

standard cell extraction means for extracting the standard cells;

logic synthesis means for conducting synthesized logic using the extracted standard cells; and

constraints and a like determination means for determining whether the logic synthesis satisfies a specification.

10. The apparatus as in claim 9, wherein

said CP aperture decision means further comprises:

CP aperture creation means for creating a new CP aperture if the CP apertures cannot satisfy the specification.

11. The apparatus as in claim 7, wherein

said placement and routing means calculates wiring routes among the placed standard cells.

12. The apparatus as in claim 7, further comprising:

first standard cell library recording means for recording magnitudes, functions and performances of the standard cells, an identification code of one of the CP apertures on which the shaping holes having the shapes of the standard cells are formed and the first placement positions, and for providing the recorded magnitudes, functions and performances of the standard cells, the identification code and the first placement positions to said CP aperture decision means.

13. The apparatus as in claim 7, further comprising:

second standard cell library recording means for recording shapes and magnitudes of outlines of the standard cells, positions of input and output signals, an identification code of one of the CP apertures on which the shaping holes having the shapes of the standard cells are formed and the first placement positions, and for providing the recorded shapes and magnitudes of the outlines of the standard cells,

positions of the input and output signals, identification code and the first placement positions to said placement and routing means.

14. The apparatus as in claim 13, further comprising:

pattern data recording means for recording the second placement positions, the identification code and wiring routes among the standard cells provided from said placement and routing means.

15. An exposure pattern data generation method for delineating patterns of systems on substrates to describe the systems in logic expressions, to convert the logic expressions into connections of standard cells, and to delineate patterns of the standard cells on the substrates, comprising:

creating Character Projection (CP) apertures having shaping holes corresponding to one hundred or more characters having shapes of the standard cells;

recording a standard cell library having an information configured to design the patterns of the systems by using the standard cells having functions, shapes of outlines, and input/output positions of the standard cells, and recording the standard cell library having first placement positions of the shaping holes on said CP apertures related to the standard cells corresponding to the shaping holes;

conducting logic synthesis for the Character Projection (CP) apertures using only the standard cells corresponding to the shaping holes placed at first placement

positions on the respective CP apertures on the substrate based on the standard cell library;

selecting one of the CP apertures for which the logic synthesis is conducted by using only the standard cells on the one of the CP apertures, which satisfies designated constraints of the systems, and which has the highest throughput in delineating one of the patterns of the systems on the substrates by using only the standard cells on the one of the CP apertures;

conducting logic synthesis again for the respective CP apertures without a constraint on using only the standard cells on the one of the CP apertures;

selecting one of the CP apertures, for which the logic synthesis is conducted again, and which has a throughput higher than a desired throughput in delineating one of the patterns of the systems on the substrates from the CP apertures on the substrates based on the standard cell library;

calculating second placement positions of the standard cells on the substrates, the standard cells corresponding to the shaping holes provided on the selected one of the CP apertures on the substrates based on the standard cell library; and

recording second placement positions of the standard cells on the substrates, the second placement positions associated with the standard cells corresponding to the first placement positions on one of the selected CP apertures.

16. The method as in claim 15, further comprising:

converting data into data capable of being used by an exposure to conduct variable shaped beam (VSB) exposure to the standard cells which cannot be subjected to exposure using the shaping holes.

17. The method as in claim 15, wherein

said conducting logic synthesis for CP apertures using standard cells corresponding to shaping holes placed at first placement positions on the respective CP apertures comprises:

extracting the standard cells; and

conducting logic synthesis using the extracted standard cells, and

said selecting a CP aperture used for exposure from the CP apertures comprises:

determining whether the synthesized logic satisfies a specification.

18. The method as in claim 15, wherein

said conducting logic synthesis for CP apertures using standard cells corresponding to shaping holes placed at first placement positions on the respective CP apertures further comprises:

creating a new CP aperture if the CP apertures cannot satisfy the specification.

19. The method as in claim 15, wherein

the calculating second placement positions of the standard cells on a substrate, the standard cells corresponding to the shaping holes provided on the selected CP aperture further comprises:

calculating wiring routes among the placed standard cells.

20. The method as in claim 15, further comprising:

recording magnitudes, functions, outline shapes and outline magnitudes of the standard cells, positions of input and output signals, identification codes of the CP apertures on which the shaping holes having the shapes of the standard cells are formed and the first placement positions.

21. The method as in claim 15, further comprising:

recording the second placement positions, identification codes and wiring routes among the standard cells.

22. The exposure as in claim 1, wherein

the standard cells on the CP apertures are listed in an order of a frequency of using each of the standard cells used by the systems, and

in an order according to a difference between a variable shaped beam (VSB) shot number, defined as a number of exposures of a one of the standard cells with VSB

exposure, and a CP shot number, defined as a number of exposures of the one of the standard cells with CP exposure.

23. The exposure as in claim 1, wherein said CP aperture decision means further comprises:

a CP aperture creation means for listing the standard cells in an order of frequency of use of each of the standard cells used by the systems, and in an order according to a difference between a variable shaped beam (VSB) shot number, defined as a number of exposures of a one of the standard cells with VSB exposure, and a CP shot number, defined as a number of exposures of the one of the standard cells with CP exposure; and

means for creating a new CP aperture based on the listed standard cells if the CP apertures cannot satisfy the desired throughput.

24. The exposure as in claim 1, wherein

the systems are logic products, and

the standard cells have shapes of the characters having shapes corresponding to the shaping holes are circuits having functions making logic expressions for logic synthesis.

25. The exposure as in claim 1, wherein

the standard cells on the CP apertures are listed in effective order of CP effectiveness defined as a quotient of a product divided by a CP shot number defined as a number of exposures of the one of the standard cells with CP exposure, the product being a result of multiplying a frequency of use of each of the standard cells used by the systems by a difference between a number of variable shaped beam (VSB) shots, defined as a number of exposures of a one of the standard cells with VSB exposure, and the CP shot number.

26. The exposure as in claim 1, further comprising:

variable shaped beam (VSB) exposure data conversion means for converting data into data capable of being used for an exposure to conduct VSB exposure of the standard cells which cannot be subjected to exposure using the shaping holes.

27. The apparatus as in claim 7, wherein

the standard cells on the CP apertures are listed in an order of a frequency of using each of the standard cells used by the systems, and

in an order according to a difference between a variable shaped beam (VSB) shot number, defined as a number of exposures of a one of the standard cells with VSB exposure, and a CP shot number, defined as a number of exposures of the one of the standard cells with CP exposure.

28. The apparatus as in claim 7, wherein

the systems are logic products, and

the standard cells have shapes of the characters having shapes corresponding to the shaping holes are circuits having functions making logic expressions for logic synthesis.

29. The apparatus as in claim 7, wherein:

the standard cells on the CP apertures are listed in effective order of CP effectiveness defined as a quotient of a product divided by a CP shot number defined as a number of exposures of the one of the standard cells with CP exposure, the product being a result of multiplying a frequency of use of each of the standard cells used by the systems by a difference between a number of variable shaped beam (VSB) shots, defined as a number of exposures of a one of the standard cells with VSB exposure, and the CP shot number.

30. The method as in claim 15, further including:

listing the standard cells on the CP apertures in an order of a frequency of using each of the standard cells used by the systems; and

listing the standard cells according to a difference between a variable shaped beam (VSB) shot number, defined as a number of exposures of a one of the standard cells with VSB exposure, and a CP shot number, defined as a number of exposures of the one of the standard cells with CP exposure.

31. The method as in claim 15, wherein said selecting further comprises:

listing the standard cells in order of frequency of use of each of the standard cells used by the systems;

listing the standard cells according to a difference between a variable shaped beam (VSB) shot number, defined as a number of exposures a one of the standard cells with VSB exposure, and a CP shot number, defined as a number of exposures of the one of the standard cells with CP exposure; and

creating a new CP aperture based on the listed standard cells if the CP apertures cannot satisfy the desired throughput.

32. The method as in claim 15, wherein the systems are logic products, and the standard cells have shapes of the characters having shapes corresponding to the shaping holes are circuits having functions, the method further including:

making logic expressions for logic synthesis using the standard cells.

33. The method as in claim 15, further comprising:

listing the standard cells on the CP apertures in effective order of CP effectiveness defined as a quotient of a product divided by a CP shot number defined as a number of exposures of the one of the standard cells with CP exposure, the product being a result of multiplying a frequency of use of each of the standard cells used by the systems by a difference between a number of variable shaped beam (VSB) shots,

defined as a number of exposures of a one of the standard cells with VSB exposure, and the CP shot number.

34. The exposure as in claim 4, wherein

the logic products are at least one of application specific ICs and system LSIs, and

the standard cells having shapes of the characters having shapes corresponding to the shaping holes are at least one of an AND circuit, a flip-flop circuit, and an inverter.

IX. EVIDENCE APPENDIX

NONE

X. RELATED PROCEEDINGS APPENDIX

NONE